***Amendments***

***In the Specification***

Please enter the following amendments:

Page 1, line 23 through Page 2, line 1, please replace the paragraph as follows:

A1

To manufacture the liquid crystal display, deposition, photolithography and etch steps are required to form the gate wire, the data wire, the gate insulating layer, the passivation layer and the pixel electrodes.

Page 2, line 2-10, please replace the paragraph as follows

A2

There are two general methods for depositing a thin film, a chemical vapor deposition (CVD) and a physical deposition. The CVD forms the film by the reaction of vaporized chemicals that contain the required constituents, while a sputtering which is a kind of physical deposition obtains the film by having energetic particles to strike target to be sputtered physically. The CVD is generally used to form the semiconductor layer and insulating layers such as the gate insulating layer and the passivation layer, and the sputtering is used to form metal layers for the gate wire and the data wire and an ITO layer for the pixel electrodes.

Page 3, lines 7-9, please replace the paragraph as follows:

A3

Because the wires according to the present invention have a low etch rate for the ITO etchant including strong acid, the chances of wire disconnection are reduced.

Page 5, lines 6 through 11, please replace the paragraph as follows:

A gate insulating layer 300 covers the gate wire 200, 210 and 230, a hydrogenated amorphous silicon (a-si:H) layer 400 and a doped hydrogenated amorphous silicon layer 410 and 420 including N type impurity are sequentially formed on the gate insulating layer 300 opposite the gate electrode 210, and the portions 410 and 420 of the doped amorphous silicon layer are opposite each other with respect the gate electrode 210.

Page 5, line 20 through Page 6, line 1, please replace the paragraph as follows:

A supplementary data wire 550 made of either molybdenum nitride or molybdenum alloy nitride is formed under the data wire 500, 510 and 520. The molybdenum alloy used in this embodiment comprises one selected from tungsten, chromium, zirconium, and nickel of the content of 0.1 to less than 20 atm %. The supplementary data wire 550 may be located on the data line 500.

Page 6, lines 2-12, please replace the paragraphs as follows:

A passivation layer 600 is formed on the data wire 500, 510 and 520 and portions of the amorphous silicon layer 400 which is not covered by the data wire 500, 510 and 520. The passivation layer 600 has a contact hole C1 exposing the drain electrode 520, and another contact hole C2 exposing the gate pad 230 along with the gate insulating layer 300. Here, the description of a data pad connected to the data line 500 is omitted.

Finally, a pixel electrode 700 formed of ITO (indium tin oxide) and connected to the drain electrode 520 through a contact hole C1 is formed on the passivation layer 600. Furthermore, a gate ITO layer 710 connected to the gate pad 230 through the contact hole

Q4 cont. C2 and improving the contact characteristic is formed on the passivation layer 600.

Page 6, lines 15-17, please replace the paragraph as follows:

Q7 Figs. 4A-4F show cross sectional views of the intermediate structures of the TFT array panel shown in Fig. 1 to Fig. 3 manufactured by a manufacturing method according to the embodiment of the present invention.

Page 6, line 18 through Page 7, line 4, please replace the paragraph as follows:

Q8 As shown in Fig. 4A, a nitride layer 251 made of either molybdenum nitride or molybdenum alloy nitride is deposited on a transparent insulating substrate 100 by using a reactive sputtering method. The target for the reactive sputtering is made of either molybdenum and molybdenum alloy having one selected from tungsten, chromium, zirconium, and nickel of the content ratio of 0.1 to less than 20 atm %. A reactive gas mixture includes argon gas (Ar) and nitrogen gas ($N_2$), and the inflow amount of the nitrogen gas is no smaller than a half of argon gas. Thereafter, a metal layer 201 made of either molybdenum or molybdenum alloy is deposited by sputtering. The metal layer 201 may be deposited before the deposition of the nitride layer 251.

Page 7, lines 10-23, please replace the paragraph as follows:

Q9 As shown in Fig. 4C, a gate insulating layer 300 made from silicon nitride, a hydrogenated amorphous silicon layer and an extrinsic or doped hydrogenated amorphous silicon layer highly doped with N type impurity are sequentially deposited by plasma-enhanced chemical vapor deposition (PECVD hereafter). The amorphous silicon layer and the extrinsic amorphous silicon layer are patterned by photolithography to form an

active pattern 401 and 411. A nitride layer 551 made of either molybdenum nitride or molybdenum alloy nitride with the thickness of 300~1,000 Å is deposited by using reactive sputtering method, and a metal layer 501 made of either molybdenum or molybdenum alloy with the thickness of 1,000 - 4,000 Å is deposited. The metal layer 501 may be deposited before the deposition of the nitride layer 551. When the thickness of the nitride layer 551 is less than 300 Å, it is difficult to obtain the uniform thickness, and the thickness of more than 1,000 Å affects the following etch step.

Page 8, lines 1-8, please replace the paragraph as follows:

As shown in Fig. 4D, the metal layer 501 and the nitride layer 551 are sequentially patterned to form a data wire including a data line 500, a source electrode 510, a drain electrode 520, a data pad (not shown), and a supplementary wire 550 by performing wet-etch using the above-described aluminum etchant. Because the etch rate for the upper metal layer 501 is higher than the etch rate for the low nitride layer 551, the metal layer 501 may be over-etched. Accordingly, it is desirable that the thickness of the nitride layer 551 is less than 1,000 Å to prevent the over-etch of the metal layer 501.

Page 8, lines 9-12, please replace the paragraph as follows:

Thereafter, exposed portions of the doped amorphous silicon layer 411 is removed to divide the doped amorphous silicon layer into two portions of 410 and 420, and the central portion of the amorphous silicon layer 400 is exposed.

Page 8, lines 16 – 22, please replace the paragraph as follows:

Finally, an ITO layer is deposited and patterned to form a pixel electrode 700

connected to the drain electrode 520 through the contact hole C1 and a gate ITO layer 710 connected to the gate pad 230 through the contact hole C2 as shown in Fig. 4F. Here, the etchant for the ITO layer comprises hydrochloric acid and nitric acid, which may penetrate along the crack of the passivation layer 600 or along the edges of the ITO wire 700 and 710, and then may reach the data wire 500, 510 and 520, and the gate pad 230.

Page 8, line 23 through Page 9, line 4, please replace the paragraph as follows:

However, because the supplementary gate wire 250 and the supplementary data wire 550 have a low chemical reaction against the ITO etchant, the gate wire 200, 210 and 230, and the data wire 500, 510 and 520 through the supplementary gate wire 250 and the supplementary data wire 550 are not disconnected.

Page 9, lines 5 – 9, please replace the paragraph as follows:

Next, the etch rate of a molybdenum-tungsten alloy nitride layer as function of volume of nitrogen gas as a reactive gas for aluminum and ITO etchants is described to confirm the low chemical reaction of the supplementary gate and data wires 250 and 550 for aluminum and ITO etchants.

***In the Claims:***

Please amend claims 4, 14, 16 and 17 as follows:

4. (Amended) A wire for a liquid crystal display, comprising:

a wire layer made of either molybdenum or molybdenum alloy;

a supplementary layer located either on or under said entire wire layer and made